

Features

- Freq. range : 1MHz to 156.25MHz
- SMD seam sealing ceramic package
- Supply voltage : 1.8V, 2.5V, 3.3V
- CMOS output
- Operating Temperature : -40°C~+105°C
- Phase Jitter : 1ps (Max.) @100MHz, 3.3V
- Dimensions : 1.6 x 1.2 x 0.6 mm
- RoHS & REACH compliant, Pb-free, Halogen-free

Applications

- NB, PC, Tablet, Smartphone, IPC, Server, Storage, Ethernet, PC peripherals, USB...etc.
- Audio ADC, Video, CPLD, FPGA, AI Vision Processing Unit, CPU, GPU, MCU, BMC...etc.

Electrical Characteristics

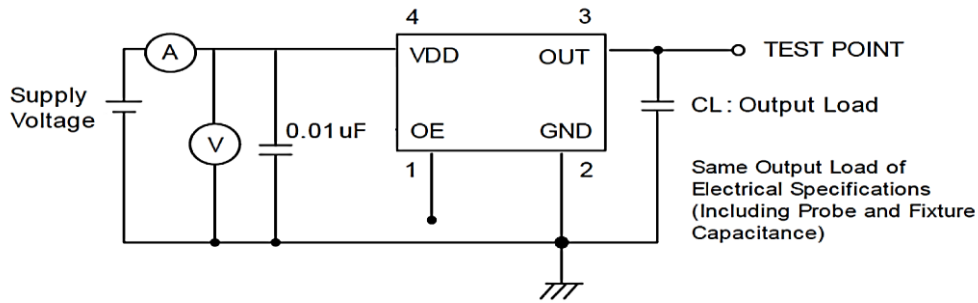
Item	8R	Conditions
Frequency Range (F ₀)	1MHz ~ 156.25MHz	V _{DD} @ 2.5 or 3.3V
	1MHz ~ 125MHz	V _{DD} @ 1.8V
Frequency Stability (F _{stab})	±25 ppm	-40°C ~ +85°C; Note[1]
	±50 ppm	-40°C ~ +105°C; Note[1]
Operating Temperature Range (T _{OTR})	-40°C ~ +85°C	
	-40°C ~ +105°C	
Supply Voltage (V _{DD})	1.8V, 2.5V, 3.3V	V _{DD} ± 10%
Current Consumption (I _{DD})	25 mA Max.	
Standby current (I _{DD-ST})	10 µA Max.	OE = Low
Output Type / Load (C _L)	CMOS / 15 pF	
Output Voltage High (V _{OH})	90% V _{DD} Min.	V _{DD} @ 2.5 or 3.3V
	(V _{DD} - 0.4V) Min.	V _{DD} @ 1.8V
Output Voltage Low (V _{OL})	10% V _{DD} Max.	V _{DD} @ 2.5 or 3.3V
	0.4V Max.	V _{DD} @ 1.8V
Rise & Fall Time (T _r / T _f)	5 ns Max.	10% ~ 90% of V _{DD} level
Duty Cycle	45% ~ 55%	
Start-up Time (T _{OSC})	10 ms Max.	To 90% of final amplitude
Enable Voltage High (VIH), Logic "1"	70% V _{DD} Min.	Enable control @ Pin 1
Enable Voltage Low (VIL), Logic "0"	30% V _{DD} Max.	
Aging (F _{aging})	±3 ppm Max.	First year at 25°C
RMS Phase Jitter (PJ) ^[2] Fout range : 10MHz~40MHz @ Integrated from 12kHz~5MHz	1.0 ps Max.	
RMS Phase Jitter (PJ) ^[2] Fout range : 40MHz~156.25MHz @ Integrated from 12kHz~20MHz	1.0 ps Typ.	

Notes:

[1] Inclusive of frequency tolerance at 25°C, variation over temperature, supply voltage variation, aging and vibration.

[2] Phase Jitter will be slightly different according to output frequency and supply voltage.

Testing diagram:

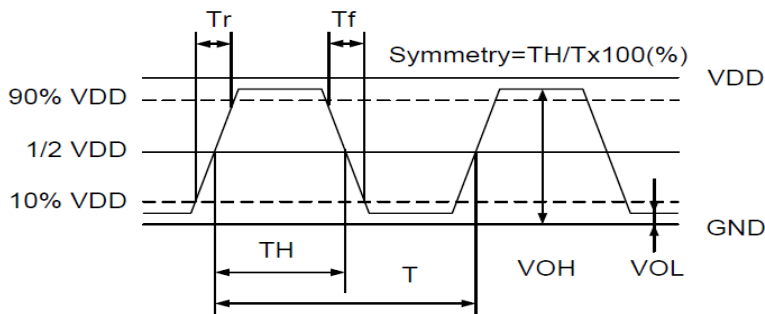


Pad 1 (OE)	Pad 3 (Output)	Oscillator
High (or open)	OSC out	Normal operation
Low	High impedance	Stop oscillation

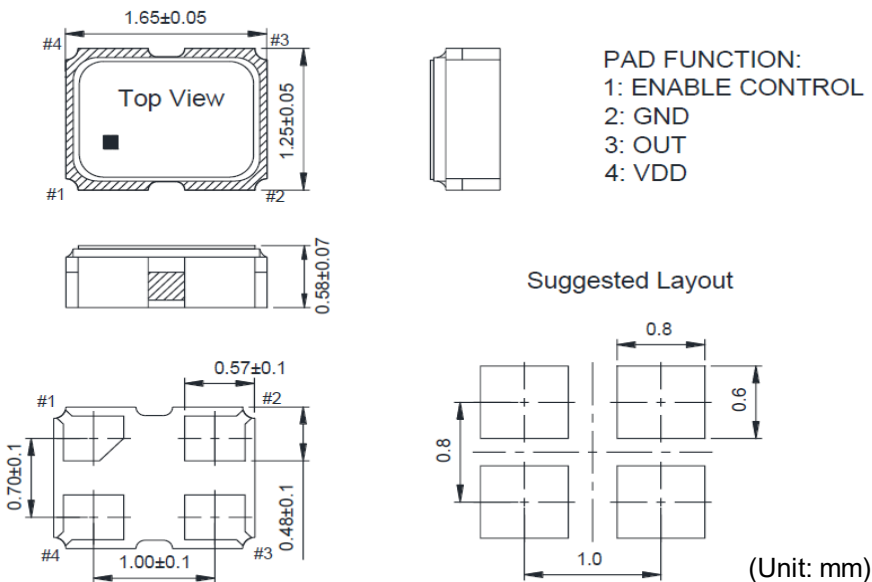
Notes: Sets CL to 15pF for simulation IC load. Customer does not need to layout it in reality circuit.

Waveform conditions :

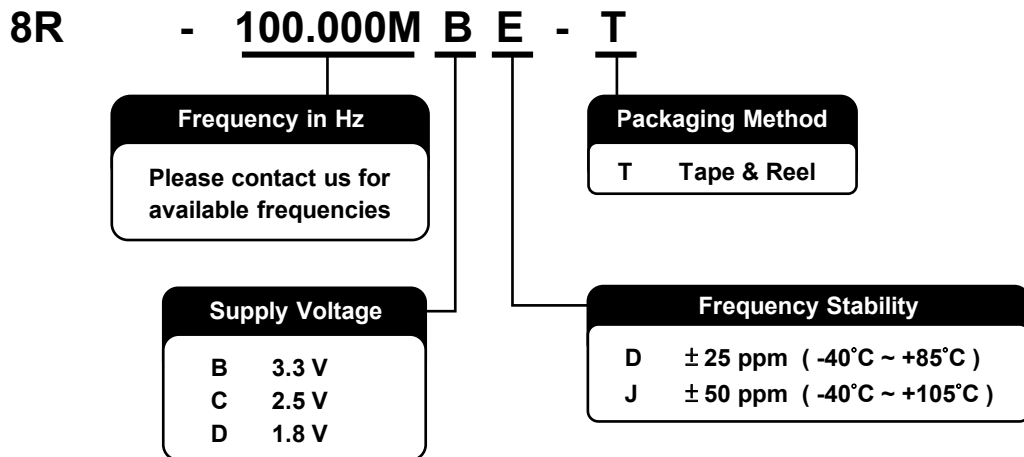
Waveform measurement system should have bandwidth min. 5 times of the frequency being tested.



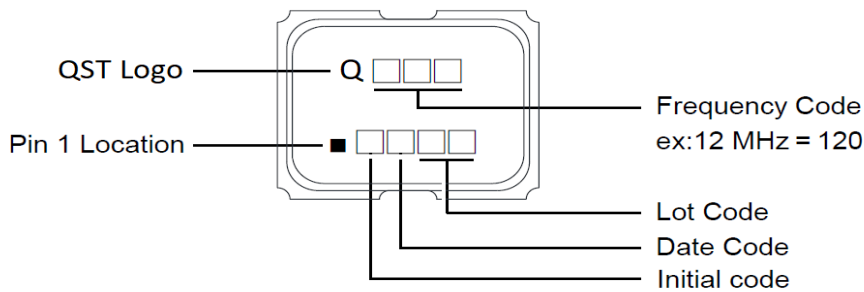
Dimensions & Recommended Footprint



Ordering Information



Marking

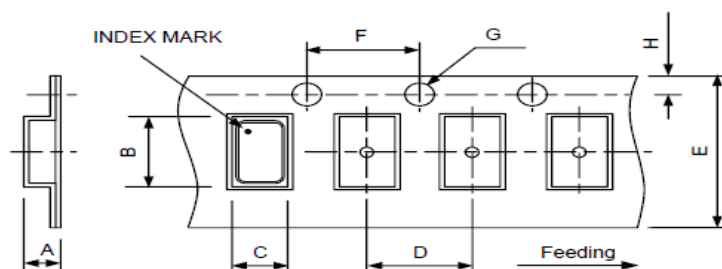


Date Code:

YEAR		MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
		2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z		
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m		
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z		

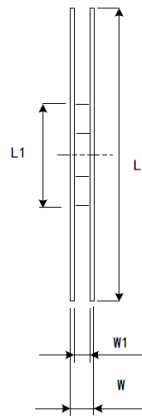
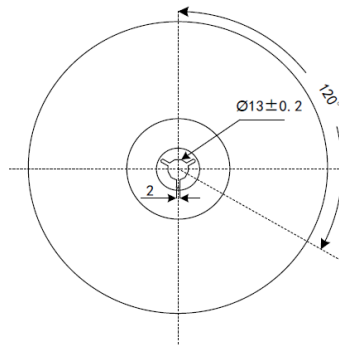
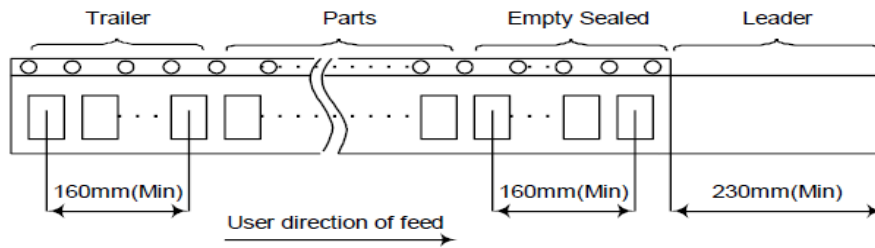
*This date code will be cycled every four years

Packing



DIMENSIONS	A	B	C	D	E	F	G	H	UNIT : mm
	0.80	1.80	1.40	4.00	8.00	4.00	1.55	1.75	

Packing



(Unit: mm)

DIMENSIONS	L	L1	W	W1	pcs / Reel (UNIT : mm)
	178	13	11.5	8	Standard Reel Quantity is 3,000 pcs per reel

Reflow Profile

Total time : 600 sec. Max.
Solder melting point : 220°C

